Short Papers

Uniplanar Broad-Band Push–Pull FET Amplifiers

Pang-Cheng Hsu, Cam Nguyen, and Mark Kintis

***Abstract*—We report the development of completely uniplanar broad-band balanced push–pull FET amplifiers using slot line and coplanar waveguide. The amplifiers employ broad-band uniplanar baluns to achieve the push–pull function over a wide bandwidth. One amplifier, designed in the unconditionally stable region, exhibits a gain of 3.5–5 dB over the frequency range of 5.4–10 GHz and an output 1-dB compression point of 19 dBm at 10 GHz. The other amplifier was designed in the potentially unstable range and achieves a high gain between 10–11 dB from 2 to 4 GHz and an output 1-dB compression point of 17 dBm at 4 GHz. These results show the feasibility of the push–pull FET amplifier configuration using uniplanar technology for microwave and millimeter-wave integrated circuits and systems.**

***Index Terms*—Amplifiers, MIC's, MMIC's, push–pull amplifiers, uniplanar circuits.**

I. Introduction

The microwave push–pull FET amplifier is attractive for many system applications because of its advantages, such as less distortion and more output power. Implementation of the push–pull configuration using uniplanar technology is very desirable for microwave and millimeter-wave integrated circuits (MIC's) and monolithic microwave integrated circuits (MMIC's), as it can create a high-performance low-cost compact amplifier.

In this paper, we report for the first time the development of two new uniplanar balanced push–pull amplifiers employing GaAs MESFET's, coplanar waveguide (CPW), and slot line. Wide-band uniplanar baluns were used to achieve the push–pull characteristics over broad-bandwidths. The first amplifier was designed in the unconditionally stable frequency range with a measured gain between 3.5–5 dB over 5.4–10 GHz. The measured output 1-dB compression point is 19 dBm at 10 GHz. The other amplifier was designed in the potentially unstable frequency range and achieved a high gain between 10–11 dB from 2 to 4 GHz. Its measured output 1-dB compression point is 17 dBm at 4 GHz.

II. Push–Pull Amplifier Theory

Fig. 1 shows a push–pull configuration consisting of a pair of FET's and two baluns. The input signal, fed to the balun, is split into two signals with equal amplitude and 180° out of phase to the gates of the FET's. The output signals from the drains of the FET's, which are equal in magnitude but differ in phase by 180°, are combined via the output balun.

The input voltages applied to the gates (as seen in Fig. 1) can be described in the forms $V_{i1} = V_m \cos wt$ and $V_{i2} = -V_m \cos wt$. The output voltages, V_{o1} and V_{o2}, of these FET's can be expressed

Manuscript received March 12, 1996; revised August 22, 1997. This work was supported by TRW, Inc.

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Publisher Item Identifier S 0018-9480(97)08248-3.

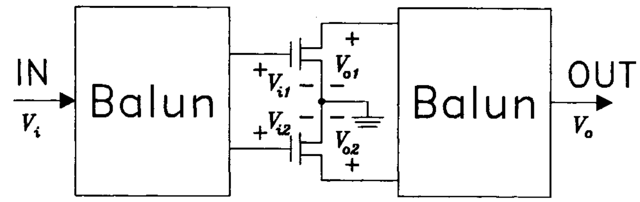

Fig. 1. Push–pull amplifier.

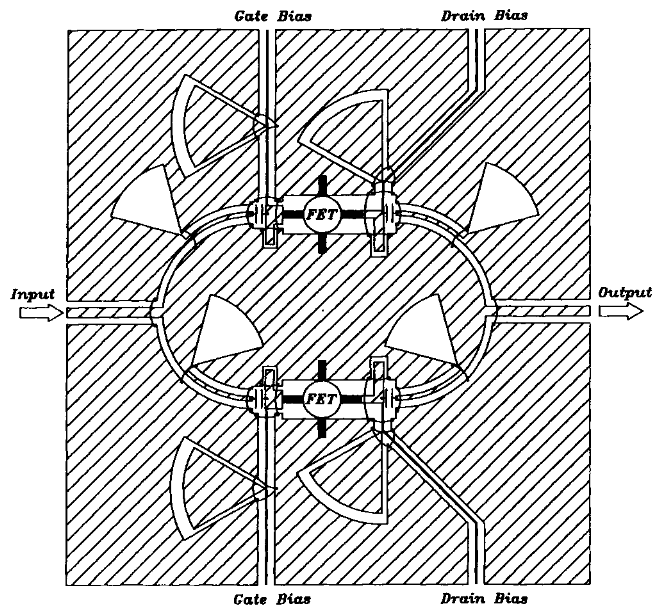

Fig. 2. Circuit layout of the uniplanar push–pull FET amplifier.

as power-series expansions of V_{i1} and V_{i2}, which then yield

$$V_{o1} = A_o + A_1 \cos wt + A_2 \cos 2wt + A_3 \cos 3wt +, \cdots,$$
$$V_{o2} = A_o - A_1 \cos wt + A_2 \cos 2wt - A_3 \cos 3wt +, \cdots,$$

where the A's are constants. The total output voltage V_o is proportional to the difference between the two voltages V_{o1} and V_{o2} and, therefore, contain only odd-order terms. This proves that a push–pull circuit will balance out all even harmonics in the output and will leave the third-harmonic term as the principal source of distortion, thus possessing inherent spurious-signal rejection of even orders and less distortion. Furthermore, because no even harmonics appear in the output of a push–pull amplifier, such a circuit will give more output power per transistor for a given amount of distortion. In addition, the fact that the output voltage contains no even-harmonic terms means that the push–pull amplifier possesses "half-wave" or "mirror" symmetry, which implies that the bottom half of the amplifier, when shifted 180° along the axis, will be the mirror image of the top half. This results in a virtual ground along the axis, which can act as the RF ground and, hence, eliminates the need of using external elements to connect the FET's to the ground. This is desirable for increasing gain and bandwidth since no inductance from the FET's sources

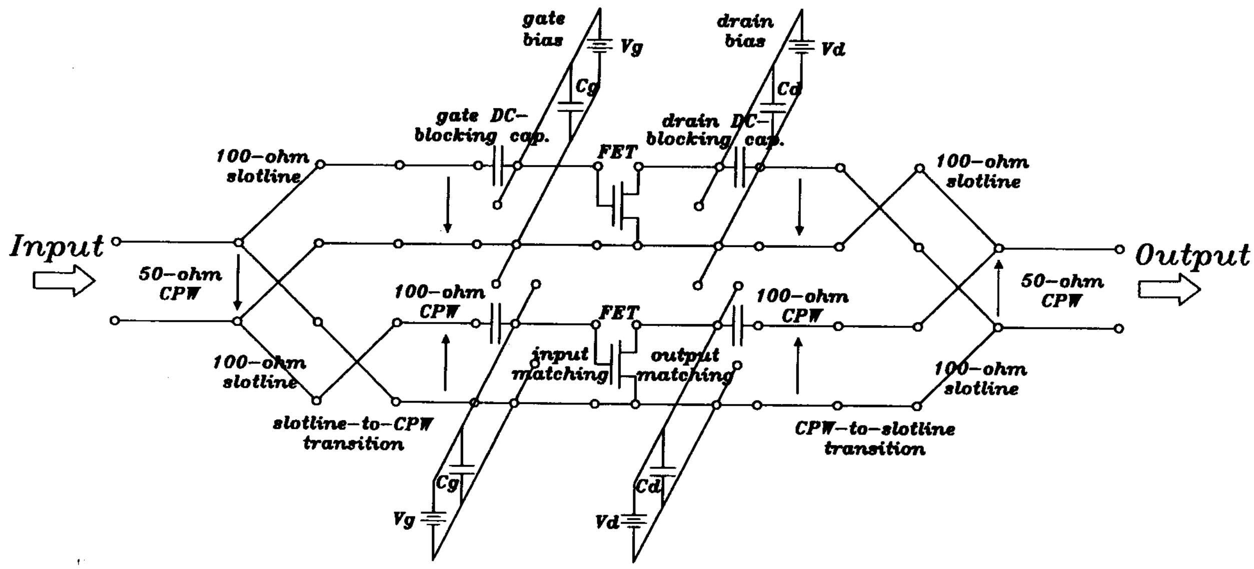

Fig. 3. Equivalent circuit of the uniplanar push–pull FET amplifier.

to the ground is encountered. It should be noted that these ideal results are obtained assuming two identical transistors. Otherwise, the appearance of even harmonics must be expected and a degradation in the circuit performance will occur.

III. Amplifier Design

Fig. 2 shows the layout of the new uniplanar push–pull balanced amplifiers. It consists of a pair of FET's, two uniplanar broadband baluns, input and output matching networks, and gate and drain biasing circuits. Each balun [1] consists of one CPW-slotline tee junction and two CPW-slotline transitions. In these baluns, the characteristic impedances of the input and output CPW's are 50 and 100 Ω, respectively, and the slot lines have a characteristic impedance of 100 Ω. Less than 0.6 dB and 3.5° in amplitude and phase balances, respectively, over an octave bandwidth were demonstrated for this kind of balun [1]. As such, we expected that these baluns provide a reasonably good balance between the two sides of each of the push–pull amplifiers; hence, less distortion and more output power can be achieved for the push–pull amplifiers as compared to their single-ended counterparts [2]. Each matching circuit consists of a CPW open-circuited stub, a cascaded CPW, and a short-circuited CPW. The short-circuited CPW is a part of the bias network, and the short is electrically achieved at the apex of the CPW open-circuited radial stub. The gate and drain biasing circuits each consists of high-impedance CPW's and a CPW open-circuited radial stub. The radial stub provides a short at its apex over the design frequency range, therefore eliminating the impedance loading effect of the biasing feed line. The FET's are mounted in a CPW arrangement, in which their sources are connected to the ground and their gate and drain are connected to the input and output matching networks, respectively. The dc blocking capacitors are located between the 100-Ω CPW's and the matching circuits, blocking the bias currents from leakage to the input and output instruments while providing a path to the high-frequency signal. The input signal is fed to the 50-Ω CPW and separated by the input balun. These signals arrive out of phase to the gates of the FET's via the dc blocking capacitors and matching circuits. The output signals are extracted from the drains of the FET's, the output matching circuits, dc blocking capacitors, output balun, and 50-Ω CPW.

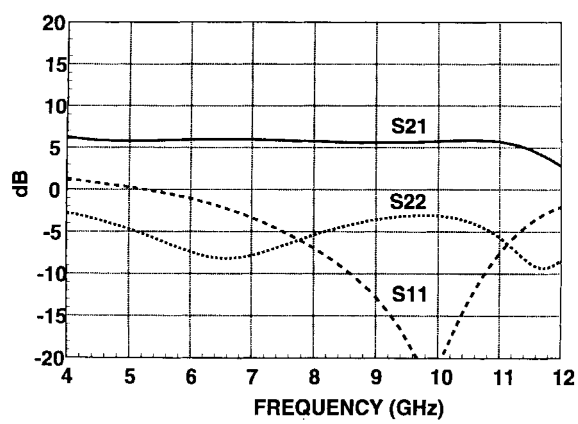

Fig. 4. Calculated gain and return losses of the 5.4–10-GHz amplifier.

We first used the commercially available LIBRA computer program[1] to design a CPW single-FET amplifier for maximum gain over the design bandwidth. This amplifier has matching circuits similar to the push–pull amplifier. We then combined two individual amplifiers through the two baluns. It should be noted here that only linear analysis was performed for the amplifiers. Fig. 3 shows the equivalent circuit of the complete amplifiers used in the design process. As LIBRA does not have models for the CPW-slotline tee junction and CPW-slotline transitions used in the baluns, we assumed these transitions behave as ideal in the simulation. The FET's used are NEC's GaAs MESFET's (NE76184AS and NE76084AS). To design the amplifiers, standard small-signal equivalent-circuit models of the FET's were obtained by using LIBRA to curve-fit the models' S-parameters to values provided in the NEC data manual.

In the first amplifier, we used NE76184AS transistors and designed the amplifier in the unconditionally stable region from 6 to 12 GHz. The other amplifier has the same circuit topology of the previous one, but with different dimensions. We also used different devices (NE76084AS), and the amplifier was designed in the potentially unstable frequency region (2–4 GHz) where a high gain is possible.

[1] LIBRA, EEsof, Westlake Village, CA 91362 USA.

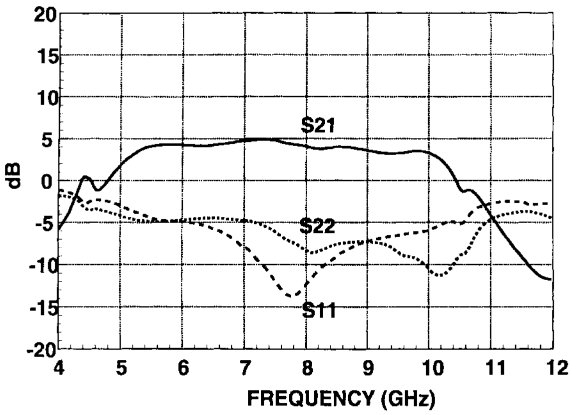

Fig. 5. Measured gain and return losses of the 5.4–10-GHz amplifier.

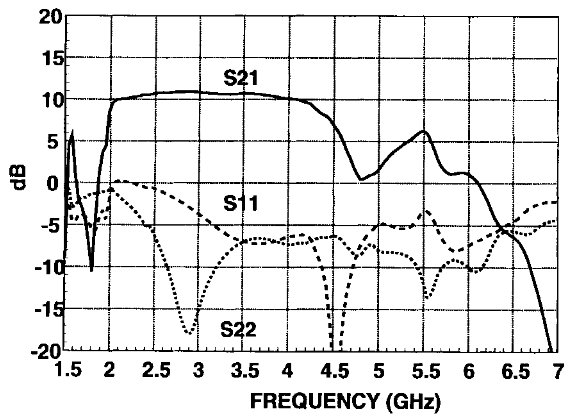

Fig. 6. Measured gain and return losses of the 2–4-GHz amplifier.

IV. Amplifier Performance

The new uniplanar push–pull amplifiers were fabricated on 1.27-mm RT/Duroid 6006, having a relative dielectric constant of 6.15. Figs. 4 and 5 show the calculated and measured gains (S_{21}) and input (S_{11}) and output (S_{22}) return losses of the first amplifier, respectively, designed using NE76184AS. The calculated magnitude of S_{11} is greater than 0 dB below 5 GHz, indicating a potential instability problem in the amplifier. This was expected as this transistor is only unconditionally stable from 6 to 11 GHz. The measured gain is between 3.5–5 dB from 5.4 to 10 GHz. Fig. 6 shows the measured gain and input and output return losses of the other amplifier using NE76084AS. The gain is between 10 and 11 dB from 2 to 4 GHz. As seen in Figs. 4 and 5, the measured and computed results for the 5.4–10 GHz amplifier are not in a good agreement. A similar discrepancy was seen for the 2–4-GHz amplifier. These discrepancies were expected because many approximations were involved in the design process; for example, the effects of the discontinuities in the uniplanar circuits and the transitions used in the baluns were not taken into account in the circuit simulations. In addition, we used the S-parameters of the FET's from the data manual which do not represent accurately the S-parameters of the actual devices used. It should be noted here that the discontinuities and transitions can be accurately modeled using full-wave methods, and the FET's used can also be accurately represented by measuring their S-parameters. These accurate models can then be used to achieve a much better agreement between the amplifiers' experimental and simulated results. However, these are beyond the scope of this paper, as our purpose is to demonstrate the feasibility of the proposed amplifier configuration. The measured output 1-dB compression points of the 2–4 GHz and 5.4–10-GHz amplifiers are 17 dBm at 4 GHz and 19 dBm at 10 GHz, respectively.

V. Conclusions

New broad-band push–pull FET amplifiers have been developed. These amplifiers employ CPW and slot line and are completely uniplanar. One amplifier exhibits a gain of 3.5–5 dB over 5.4–10 GHz and an output 1-dB compression point of 19 dBm at 10 GHz. The other amplifier has a measured gain from 10 to 11 dB over 2–4 GHz and an output 1-dB compression point of 17 dBm at 4 GHz. These amplifiers demonstrate a successful implementation of the push–pull amplifier configuration using uniplanar technology for MIC's and MMIC's.

Acknowledgment

The authors wish to thank L. Fan and M. Li for their technical support. They also are grateful to the anonymous reviewers for their valuable comments and suggestions.

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[2] S. A. Maas, *Nonlinear Microwave Circuits.* Norwood, MA: Artech House, 1988.

The Method of Lines for the Hybrid Analysis of Multilayered Cylindrical Resonator Structures

Dennis Kremer and Reinhold Pregla

***Abstract*—A very powerful numerical model based on the method of lines (MoL) is developed for the hybrid analysis of composite multilayered cylindrical dielectric resonator structures. These structures are composed of a number of coaxial rings which are arbitrarily layered in the axial direction. The resonant frequencies, as well as quality factors caused by radiation or dielectric loss and the corresponding field distributions of all resonant modes can be determined with the described algorithm. The theory is verified in case of the conical dielectric resonator and a comparison of our numerical results with those of other authors shows excellent consistency.**

***Index Terms*—Conical resonator, MoL, multilayered cylindrical dielectric resonators.**

Manuscript received June 27, 1996; revised December 1, 1996.

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Publisher Item Identifier S 0018-9480(97)08238-0.